APPLICATION NOTE

5-Volt Horizontal Clock Drivers

for use with Kodak KAI-2000, KAI-2093, KAI-4010 and KAI-4020 interline image sensors

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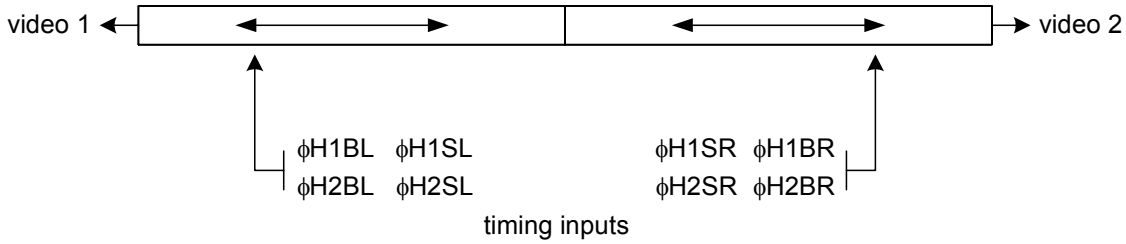
Revision 1

MTD/PS-0498 Rev. 1

www.kodak.com/go/imagers 585-722-4385 Email: imagers@kodak.com

This document describes a simple horizontal CCD clock driver for the KAI-2000, KAI-2093, KAI-4010, and KAI-4020 image sensors.

HCCD Register Operation



The horizontal CCD is arranged to allow the entire image to be read out of either video 1 or video 2 (mirror image). For faster read out both video 1 and video 2 may be used simultaneously. The horizontal shift register is designed as a reversible pseudo 2-phase CCD. The direction of charge transfer in the horizontal CCD is controlled by the wiring connections.

To direct all pixels to the video 1output, make the following HCCD connections:

ϕH1 = ϕH1SL, ϕH1SR, ϕH1BL, ϕH2BR
and
ϕH2 = ϕH2SL, ϕH2SR, ϕH2BL, ϕH1BR

where ϕH1 is the output of the H1 phase timing generator and ϕH2 is the output of the H2 phase timing generator.

To direct all pixels to the video 2 output, make the following HCCD connections:

ϕH1 = ϕH1SL, ϕH1SR, ϕH2BL, ϕH1BR
and
ϕH2 = ϕH2SL, ϕH2SR, ϕH1BL, ϕH2BR

For faster image read out, direct the left half of the image to video 1 and the right half of the image to video 2 by making the HCCD connections:

ϕH1 = ϕH1SL, ϕH1SR, ϕH1BL, ϕH1BR
ϕH2 = ϕH2SL, ϕH2SR, ϕH2BL, ϕH2BR

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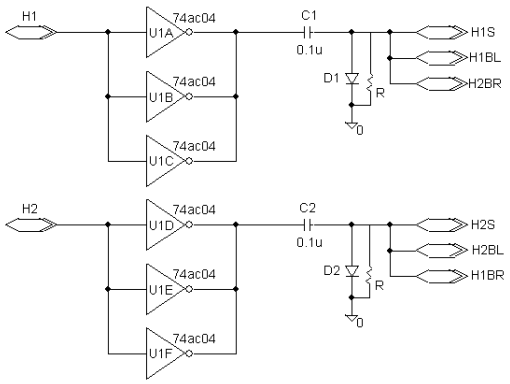
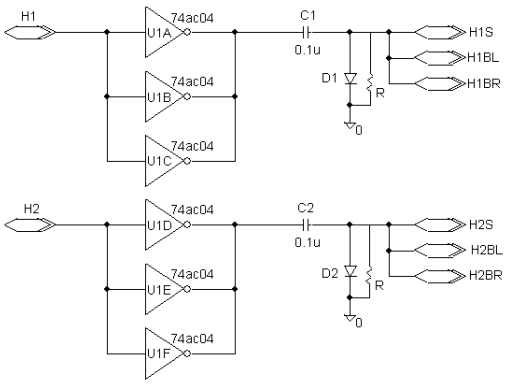
HCCD Clock Driver

The HCCD clock inputs should be driven by buffers capable of driving the sensor capacitance and having a full voltage swing of at least 4.75V. A 74AC04 or equivalent is recommended to drive the HCCD. The HCCD requires a low-level voltage in the range of – 5V to – 4V. A negative clock level is easily obtained by capacitive coupling and a diode to clamp the high level to GND.

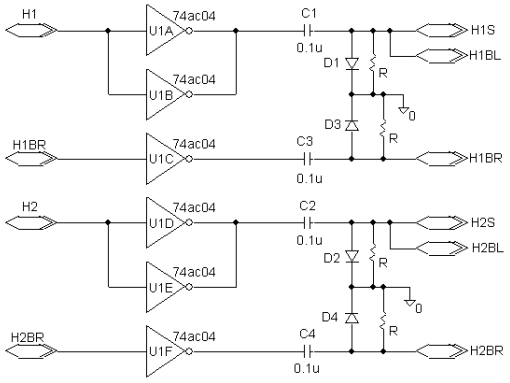
single output only



dual output only



selectable single or dual output



The inputs to the above circuits, ϕH1 and ϕH2, are 5-V logic from the timing generator (e.g., the Kodak KSC-1000 support chip or a programmable gate array). If the camera is to have selectable single or dual output modes of operation, then the timing logic needs to generate two extra signals for the ϕH1BR and ϕH2BR timing. For single output mode, program the timing such that ϕH1BR=ϕH2 and ϕH2BR=ϕH1. For dual output mode program the timing such that ϕH1BR=ϕH1 and ϕH2BR=ϕH2.

The resistor in the above circuit, R, is there to ensure the high level of the diode-clamped signal does not start up below zero volts. The value of R should be in the range of 47kΩ to 200kΩ. If the timing to the clock driver is stopped in the low level state for more than the horizontal retrace time, then the coupling capacitor will begin to

discharge through the resistor R. If the clocks are stopped during a long integration time, while no image is being read out, then stop both clocks in the high level state to prevent the capacitor from discharging.

To prevent signal cross talk (through clock edge jitter), do not mix the horizontal clock buffers in the same package as other timing signals.